Main

Welcome to the RISC-V Port Project!

RISC-V is a free and open-source RISC instruction set architecture (ISA) designed originally at the University of California, Berkeley, and now developed collaboratively under the sponsorship of RISC-V International. It is already supported by a wide range of language toolchains.

With the increasing availability of RISC-V hardware, a port of the JDK would be valuable. RISC-V ISA is actually a family of related ISAs of which there are currently four base ISAs [1]. Those base ISAs can be combined with a set of standard extensions. RV64G and RV32G are defined as general-purpose ISAs.

We have ported JDK to a new platform: Linux/RISC-V. This port supports the following subsystems:

- The template interpreter
- The C1 (client) JIT compiler
- The C2 (server) JIT compiler
- All current mainline GCs, including Z and Shenandoah

Currently, this port supports the RV64G configuration of RISC-V, which is the general-purpose 64-bit RISC-V ISA.

In addition, we have experimental support for RVV, RVC, Zba and Zbb RISC-V ISA-extentions. These features need to be explicitly enabled respectively

through: -XX:+UseRVV, -XX:+UseRVC, -XX:+UseZba and -XX:+UseZbb JVM options. In the future we may consider supporting other RISC-V configurations such as,

for example, a general-purpose 32-bit configuration (RV32G).

RISC-V port is in JDK mainline, use the regular builds if you need RISC-V JDK.

We have provided cross-build instructions for reference [2] if you want to build RISC-V JDK yourself. Hotspot disassember is also available [3].

You can try RISC-V JDK with QEMU User/System mode or hardwares like HiFive Unleashed/Unmatched board.

Have fun and happy hacking 😉

[1] https://github.com/riscv/riscv-isa-manual

[2] http://cr.openjdk.java.net/~fyang/openjdk-riscv-port/BuildRISCVJDK.md

[3] http://cr.openjdk.java.net/~fyang/hsdis/hsdis-riscv64.so

Project structure

- `master` branch - synced automatically with the master branch of openjdk/jdk
- `riscv-port branch` - for normal riscv-port project development purpose

Resources

- RISC-V Port Project
- Repository
- Mailing list: riscv-port-dev (archives)

Recent space activity

Fei Yang
Main updated Mar 31, 2022 view change

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Main updated Nov 05, 2021 view change

Space contributors

- Fei Yang (917 days ago)
- Iris Clark (1063 days ago)